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EXAMINER
WOOD, WILLIAM H

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 03/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/385,927	GRUNER ET AL.	
	Examiner	Art Unit	
	William H. Wood	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *1-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *22 July 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claims 1-37 have been examined.

Specification

1. The disclosure is objected to because of the following informalities: page 14, line 2 indicates shifter 506 contains bytes 2-13 yet it is only an eight byte shifter. The error occurs again on page 15 in table 2. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 20-25 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 20 makes reference to a *predetermined length*. However, this limitation is not found in the disclosure and appears to be a new interpretation of the disclosure, which is not readily apparent. Thus, the new limitation, which gives a new interpretation is new matter and should be removed.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 20-23, 26-27, 29-32, and 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimazawa et al. (USPN 5,646,873) in view of Brown et al. (USPN 5,600,806).

In regard to claim 20, Shimazawa disclosed the limitations:

i) determining in a length decoder and in a first clock cycle (Figure 1, element 4 and second shifter BSA1 directly connected), a length of a current code in the code stream (Figure 1, element R3A0)

ii) if the length of the current code is less than a predetermined length (predetermined length is equal to the second shift register) then shifting the code stream to a start of a successive code in the code stream based on the length of the current code (Figure 1, element 4 and data line SH1 provide shifting second shifter to start of next code), said shifting being performed during the first clock cycle (Figure 1 shows circuitry not being in different clock cycles; column 3, lines 55-60; indicate first shifter is used in next cycle)

iii) if the length of the current code is greater than the predetermined length then shifting the code stream to the start of the successive code one clock cycle later (column 3, lines 55-60; indicate first shifter is used in next cycle; if current data is larger than the second shifter it must go to the next shifter and therefore the next cycle)

Shimazawa did not explicitly state *instruction* alignment and decoding. Brown demonstrated that it was known at the time of invention to align instructions (column 2, lines 48-52). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Shimazawa's variable length code alignment as aligning instructions as found in Brown's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to provide alignment of instructions and thus allowing a processor to quickly decode and execute those instructions by knowing the proper boundaries for instruction operation information.

In regard to claim 21, Shimazawa and Brown further disclosed the limitation *wherein the shifting one clock cycle later is performed in a first shifter* (Figure 1, element R50 and add function indicate a cycle later), *and the shifting in the first clock cycle is performed in a second shifter* (Figure 1, element BSA1 has no impediments to first cycle shifting).

In regard to claim 22, Shimazawa and Brown further disclosed the limitation *wherein an output of the first shifter forms an input to the second shifter* (Figure 1, data line between two shifters).

In regard to claim 23, Shimazawa and Brown further disclosed the limitation *wherein the second shifter is connected to the length decoder via a latch* (Figure 1, element R3A0).

In regard to claim 26, Shimazawa disclosed the limitations:

i) determining a length of a first code in the code stream during a length decode stage (Figure 1, element 4)

ii) inputting the length of the first code to a two-stage code alignment stage comprising first and second shift operations performed by first and second shifters respectively (Figure 1, elements BSA0 and BSA1), wherein an output of the second shift operations comprises codes of the code stream aligned to a start of a successive code in the code stream immediately following the first code (column 3, lines 37-60 column 5, lines 8-17 and Figure 1), the output of the second shift operation defining an input to the length decode stage (Figure 1, element R3A0),

iii) and wherein if the first code is contained in the second shifter said first code is shifted into a length decoder that performed the length decode stage in the same clock cycle in which the length of the first code was determined (column 3, lines 37-60 and Figure 1; shifter provides data to length decoder and decoder sends length back to shifter in same clock cycle, lines are direct; no need for second shifter to need first shifter), and wherein if the first code is not contained in the second shifter, said first code is shifted from the first shifter one clock cycle later into the length decoder from the first shifter (column 3, lines 55-60 and Figure 1; first shifter now shifts based upon the preceding cycle; adder between length decoder and first shifter increases the clock and the second shifter did not have all of the first code)

Shimazawa did not explicitly state *instruction* alignment and decoding. Brown demonstrated that it was known at the time of invention to align instructions (column 2, lines 48-52). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Shimazawa's variable length code alignment as aligning instructions as found in Brown's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to provide alignment of instructions and thus allowing a processor to quickly decode and execute those instructions by knowing the proper boundaries for instruction operation information.

In regard to claim 27, Shimazawa and Brown did not directly state the limitation *wherein the first and second shifters are connected in series and are synchronized to the same clock cycle*. Official Notice is taken that it was known at the time of invention to implement multiple circuit elements in serial and also to implement multiple circuit elements synchronized on the same clock. It would have been obvious to one of ordinary skill in the art at the time of invention to implement Shimazawa and Brown in a manner as to have one clock and in serial. This implementation would have been obvious because one of ordinary skill in the art would be motivated to use common elements in designing the circuit disclosed by Shimazawa modified by Brown's teaching, in order to reduce cost of design.

In regard to claim 29, Shimazawa and Brown further disclosed the limitation *wherein inputting the length of the first instruction comprises inputting said length directly from the length decoder to the second shifter* (Figure 1, data line SH1).

In regard to claim 30, Shimazawa and Brown further disclosed the limitation *wherein inputting the length of the first instruction comprises inputting said length from the length decoder to the first shifter via an intermediate latch* (Figure 1, element R50).

In regard to claim 31, Shimazawa disclosed the limitations:

i) *a first shifter* (Figure 1, element BSA0)

ii) *a second shifter* (Figure 1, element BSA1)

iii) *a length decoder* (Figure 1, element 4), *wherein an output of the first shifter forms a direct input to the second shifter* (data line between two shifters), *an output of the second shifter is sent to the length decoder via an intermediate latch* (Figure 1, element R3A0), *and wherein a length of a current instruction in the length decoder is directly input into the second shifter* (Figure 1, data line SH1).

Shimazawa did not explicitly state *instruction* alignment and decoding. Brown demonstrated that it was known at the time of invention to align instructions (column 2, lines 48-52). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Shimazawa's variable length code alignment as aligning instructions as found in Brown's teaching. This implementation would have been

obvious because one of ordinary skill in the art would be motivated to provide alignment of instructions and thus allowing a processor to quickly decode and execute those instructions by knowing the proper boundaries for instruction operation information.

In regard to claim 32, Shimazawa disclosed the limitation *wherein a length of the current instruction in the length decoder is input into the first shifter via an intermediate latch* (Figure 1, element R50).

In regard to claim 35, Shimazawa disclosed the limitations:

i) *first shifting means for shifting bytes of the instruction stream* (Figure 1, element BSA0)

ii) *second shifting means for shifting bytes of the instruction stream* (Figure 1, element BSA1)

iii) *length decoding means for determining a length of an instruction in the instruction stream* (Figure 1, element 4), *wherein an output of the first shifting means forms a direct input to the second shifting means* (data line connecting the two shifting means), *an output of the second shifting means is sent to the length decoding means via an intermediate latching means* (Figure 1, element R3A0), *and wherein a length of a current instruction in the length decoding means is directly input into the second shifting means* (Figure 1, data line SH1)

Shimazawa did not explicitly state *instruction* alignment and decoding. Brown demonstrated that it was known at the time of invention to align instructions (column 2,

lines 48-52). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Shimazawa's variable length code alignment as aligning instructions as found in Brown's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to provide alignment of instructions and thus allowing a processor to quickly decode and execute those instructions by knowing the proper boundaries for instruction operation information.

In regard to claim 36, Shimazawa disclosed the limitation *wherein a length of the current instruction in the length decoder means is input into the first second shifting means via an intermediate latch means* (Figure 1, element R50).

6. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimazawa et al. (USPN 5,646,873) in view of Brown et al. (USPN 5,600,806) as applied above and in further view of Riffe et al. (USPN 4,502,111).

In regard to claim 24, Shimazawa and Brown did not explicitly state the limitation *wherein the predetermined length is 8 bytes*. Riffe demonstrated that it was known at the time of invention to have rotators/shifters of 8 bytes (Figure 1, element 41). And the physical size of a rotator/shifter is what determines the predetermined length. It would have been obvious to one of ordinary skill in the art at the time of invention to implement Shimazawa's barrel shifter/rotator with 8 bytes as found in Riffe's teaching. This implementation would have been obvious because one of ordinary skill in the art would

be motivated to utilize a common rotator size, especially one (such as in Riffe) which is used for instruction alignment based upon length.

7. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimazawa et al. (USPN 5,646,873) in view of Brown et al. (USPN 5,600,806) as applied above and in further view of Coon et al. (USPN 5,619,666).

In regard to claim 25, Shimazawa and Brown did not directly state the limitation *wherein the first shifter is able to shift 16 bytes of data*. Coon demonstrated that it was known at the time of invention to have rotators/shifters of 16 bytes (column 10, lines 24-26). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Shimazawa and Brown in a manner as having a first barrel shifter/rotator being 16 bytes. This implementation would have been obvious because one of ordinary skill in the art would be motivated to make the first shifter 16 bytes as this is a typical line size in a cache and the first rotator is closer to the cache/instruction buffer in Shimazawa's disclosed barrel shifter/rotator modified by Brown's teaching.

8. Claims 28, 33-34 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimazawa et al. (USPN 5,646,873) in view of Brown et al. (USPN 5,600,806) as applied above and in further view of Riffe et al. (USPN 4,502,111) in view of Coon et al. (USPN 5,619,666).

In regard to claim 28, Shimazawa and Brown did not directly state the limitation *wherein the first shifter has a capacity of 16 bytes and the second shifter has a capacity of 8 bytes*. Riffe demonstrated that it was known at the time of invention to have rotators/shifters of 8 bytes (Figure 1, element 41). Coon demonstrated that it was known at the time of invention to have rotators/shifters of 16 bytes (column 10, lines 24-26). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Shimazawa and Brown in a manner as having a first barrel shifter/rotator being 16 bytes and a second barrel shifter/rotator being 8 bytes. This implementation would have been obvious because one of ordinary skill in the art would be motivated by Riffe to make the rotator (second shifter) closest to the length decode and shifting 8 bytes (Riffe: Figure 1) and motivated to make the other rotator (first shifter) 16 bytes as this is a common line amount in a cache and the first rotator is closer to the cache/instruction buffer.

In regard to claim 33, Shimazawa and Brown did not directly state the limitation *wherein the first shifter has a greater shifting capacity than the second shifter*. Riffe demonstrated that it was known at the time of invention to have rotators/shifters of 8 bytes (Figure 1, element 41). Coon demonstrated that it was known at the time of invention to have rotators/shifters of 16 bytes (column 10, lines 24-26). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Shimazawa and Brown in a manner as having a first barrel shifter/rotator being 16 bytes and a second barrel shifter/rotator being 8 bytes. This implementation would have been

obvious because one of ordinary skill in the art would be motivated by Riffe to make the rotator (second shifter) closest to the length decode and shifting 8 bytes (Riffe: Figure 1) and motivated to make the other rotator (first shifter) 16 bytes as this is a common line amount in a cache and the first rotator is closer to the cache/instruction buffer.

In regard to claim 34, Shimazawa and Brown did not directly state the limitation *wherein the first shifter has a capacity of 16 bytes and the second shifter has a capacity of 8 bytes*. Riffe demonstrated that it was known at the time of invention to have rotators/shifters of 8 bytes (Figure 1, element 41). Coon demonstrated that it was known at the time of invention to have rotators/shifters of 16 bytes (column 10, lines 24-26). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Shimazawa and Brown in a manner as having a first barrel shifter/rotator being 16 bytes and a second barrel shifter/rotator being 8 bytes. This implementation would have been obvious because one of ordinary skill in the art would be motivated by Riffe to make the rotator (second shifter) closest to the length decode and shifting 8 bytes (Riffe: Figure 1) and motivated to make the other rotator (first shifter) 16 bytes as this is a common line amount in a cache and the first rotator is closer to the cache/instruction buffer.

In regard to claim 37, Shimazawa and Brown did not directly state the limitation *wherein the first shifter has a greater shifting capacity than the second shifter*. Riffe demonstrated that it was known at the time of invention to have rotators/shifters of 8

bytes (Figure 1, element 41). Coon demonstrated that it was known at the time of invention to have rotators/shifters of 16 bytes (column 10, lines 24-26). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Shimazawa and Brown in a manner as having a first barrel shifter/rotator being 16 bytes and a second barrel shifter/rotator being 8 bytes. This implementation would have been obvious because one of ordinary skill in the art would be motivated by Riffe to make the rotator (second shifter) closest to the length decode and shifting 8 bytes (Riffe: Figure 1) and motivated to make the other rotator (first shifter) 16 bytes as this is a common line amount in a cache and the first rotator is closer to the cache/instruction buffer.

Examiner's Response

9. Applicant's arguments with respect to claims 20-37 have been considered but are moot in view of the new ground(s) of rejection. Examiner responds with the above rejection.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William H. Wood whose telephone number is (703)305-3305. The examiner can normally be reached 7:30am - 5:00pm Monday thru Thursday and 7:30am - 4:00pm every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7239 for regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

William H. Wood
March 10, 2003

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